assuming an advanced self-aligned oxide-isolated 1 μm bipolar technology with an internal transistor derived from the 2·5 μm technology currently in use at the Ruhr-Universität.[5] In critical places in the circuit, 'full precision' transistors with 5 × 5 μm^2 or larger emitters were used. Critical resistors had 10 μm minimum dimensions.

Circuit details include emitter-follower input buffers, fairly conventional latched comparators and emitter function logic[6] wired-AND, wired-OR and noninverting pipeline latches. The amplifier input stages consist of simple differential pairs with emitter degeneration, all collectors being connected in parallel to the main amplifier inputs. A single current source is routed to enable one of the differential pairs. The main amplifier uses feedback to present low input impedances to the capacitively loaded input stage bus lines. In order to preserve accuracy over temperature, the end point voltages for the reference chain of ADC-2 are generated by two similar amplifiers. The total component count is about 5800.

The error budget of the ADC system includes amplifier output DC errors, linearity and common mode, of $\pm$1·4 mV (1/11 LSB) and white noise of 2·3 mV_{eff} (1/7 LSB; note that due to the wide system bandwidth, transistor flicker noise is insignificant so long as the flicker noise corner frequency is well below 1 MHz.) To allow for the other error contributions, an amplifier settling error band of 1/32 LSB was assumed. Errors due to parameter variations across the chip were not simulated. As stated above, redundancy correction is used to relieve accuracy requirements for the comparator thresholds, so the most critical error sources remaining in the system are the offset voltages of the amplifier input stages. Assuming that a technology capable of accurately defining 1 μm structures will achieve an offset voltage standard deviation of $<$0·1 mV, an acceptable yield of 12-bit linear devices can be expected (compare the remarks on transistor offset voltages in Reference 2).

Circuit simulations predict a minimum ADC cycle time of 8·4 ns, but as a sample-hold circuit is necessary in order to permit Nyquist sampling of fast-changing input signals, it is clear that this is where the speed bottleneck will be with systems of the new architecture. The authors are working on a proposal for a fast monolithic integrated 12-bit sample-hold circuit. The fastest commercial high-precision sample-hold circuit known to the authors is a hybrid[7] that would add about 24 ns to the above value, resulting in a total system cycle time of 33 ns, or a maximum conversion rate of 30 megasamples per second. See Table 1 for a summary of system data.

Table 1 ADC EXAMPLE EXPECTED DATA

Resolution	12 bits
Input voltage range	2 V
Component count	5800
Number of precision components	790
ADC cycle time	8·4 ns
System cycle time incl. s–h[7]	33 ns

Comparison to other fast ADC system architectures: With similar circuitry, the same technology, and about the same power consumption, a comparison simulation of a conventional parallel-serial feedforward ADC with DAC and summing point predicts an ADC cycle time of 21 ns (2·5 times that of the new architecture), or a 45 ns system cycle including the sample-hold example of above. While its total component count is only 16% below that of the new system, it does use considerably less 12-bit precision components, only about 27 against 790.

The all-parallel ADCs need such prohibitively high numbers of full-precision components—at 12-bit resolution about 8300 in case of the two-step parallel ADC of Reference 3 and almost 25 000 for the flash ADC—that their application to systems of much more than 10 bits of resolution seems very unlikely. Note that with both all-parallel structures, redundancy correction is not available as a means to relieve accuracy requirements even for parts of the system. At 12 bits, they are also slower: in the case of the flash ADC, because the 2 W power limit for monolithic integration leaves its 4095 comparators each with only 1/13 the power of the simulated comparators, and in the case of the two-step parallel ADC, because the track-to-hold settling time of the sample-hold increases due to the absence of redundancy correction.

Conclusions: A new architectural option for the speed-complexity tradeoff of high-speed high-resolution ADCs has been presented. With its help, it should be possible to extend high-speed capabilities to resolutions where the all-parallel approaches become impractical for reasons of yield and complexity. However, to put the full speed of this structure to system use, sample-and-hold performance levels will have to be pushed way beyond the present state-of-the-art.

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G. STEINBACH
U. LANGMANN

Institut für Elektronik
Ruhr-Universität Bochum
D-4630 Bochum, W. Germany

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OPTICAL FLIP-FLOP

Indexing terms: Optoelectronics, Optical logic

The operation of a clocked optical S-R flip-flop, based on a polarisation-bistable semiconductor laser, is demonstrated.

A digital optical computation system must store binary optical signals in addition to performing optical logic operations. The basic building blocks of a digital system are logic gates and flip-flops, in which the gates perform the logic and the flip-flops perform memory functions. In conventional electronic systems, the flip-flops are constructed by combining many logic gates with complicated circuitry. In this letter we present the operation of an optical flip-flop with very simple circuitry based on polarisation bistability[1] in semiconductor lasers which we have recently observed.

The polarisation-bistable lasers are V-grooved substrate buried heterostructure InGaAsP/InP lasers emitting at 1·3 μm wavelength. When the laser is operated in its characteristic polarisation transition temperature regime,[2] the polarisation-resolved CW power/current characteristics of the laser exhibit remarkable hysteresis, as shown in Fig. 1. The light output can be switched between the two polarisation states by injection of short electrical or optical pulses.[1] With the polarisation-bistable laser and a few optoelectronic switches[3,4] or photodetectors, we have demonstrated the operations of clocked optical flip-flops based on the characteristics described above. Unlike conventional electronic or optical flip-flops, our optical flip-flops are not constructed by combining logic gates. The simplicity of the circuitry is a great advan-

tage for monolithic integration and high-speed applications. Since the laser changes states by switching between the TE and TM modes, the switching behaviour of one mode is always complementary to that of the other, and the output

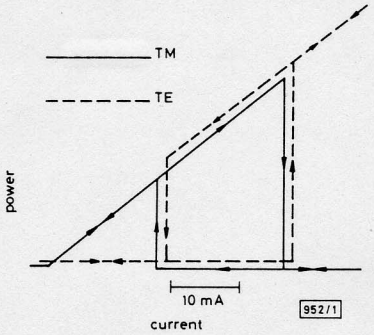

Fig. 1 *Polarisation-resolved CW power/current characteristics of a polarisation-bistable semiconductor laser*

Origin of TE curve is shifted for clarity. Note that injection current is negative

signals from the same laser in each of the two orthogonal polarisations directly constitute the normal output Q and its complement $\bar{Q}$, respectively. This special feature is certainly not available in conventional intensity-bistable semiconductor lasers.[5] It reduces the number of components in a flip-flop as no extra components for generating the complement output are necessary.

We present in the following a basic optical S-R flip-flop to demonstrate the full capability of our schemes. Fig. 2*a* shows the proposed circuit of an S-R flip-flop consisting of three high-speed optoelectronic switches (OS) and a polarisation-bistable laser diode (LD) which is biased in the middle of the hysteresis loop. Two switches are used as the input ports of the flip-flop to receive the digital optical input signals, S and R. A third switch, activated by a train of optical clock pulses CP, is used to sample the output of the first two switches in synchronism with the clock pulses. The output pulses from this switch then trigger the laser diode to switch the polarisation of its output at the repetition rate of the clock pulses. As previously discussed, the TE and TM outputs constitute the normal output Q and its complement $\bar{Q}$, respectively. In the absence of a clock pulse, changes in logic state at the data input cause no change in the output. At the moment a clock pulse arrives, if $S = 0$ and $R = 0$, no voltage is applied to the third switch and there is no sampled output pulse to trigger the laser. The laser stays in its previous state Q_n. If $S = 0$ and $R = 1$ at the moment of a clock pulse, a positive output pulse propagates through the third switch. The laser output is switched from TE to TM. If the laser originally operates in the TM mode, it stays in the TM mode at the triggering of a positive pulse. Therefore, the condition $S = 0$ and $R = 1$ always results in $Q_{n+1} = 0$ ($\bar{Q}_{n+1} = 1$). If $S = 1$ and $R = 0$, a negative pulse is sampled. The laser is triggered to operate in the TE mode ($Q_{n+1} = 1$). The condition $S = 1$ and $R = 1$ is forbidden in conventional electronic S-R flip-flops because it results in an indeterminate state as indicated by the question mark in Fig. 2*c*. However, in our optical S-R flip-flop, we have experimentally observed that, when the two input ports are well balanced, the condition $S = 1$ and $R = 1$ generates $Q_{n+1} = Q_n$ and is not indeterminate. The logic diagram and the characteristic table of the S-R flip-flop are shown in Fig. 2*c*.

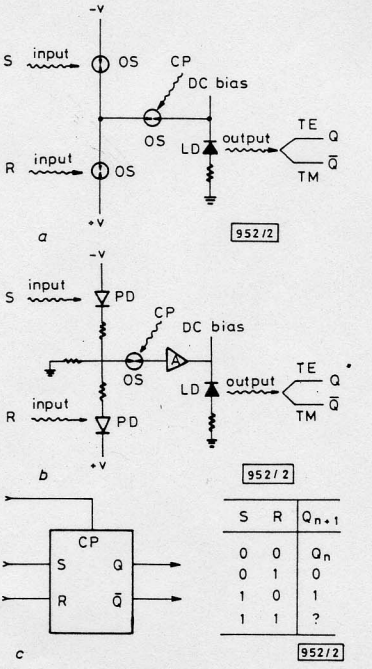

Fig. 2

a The circuit of an optical S-R flip-flop consisting of three optoelectronic switches

b An alternative circuit using two photodetectors. PD is the photodetector, OS the optoelectronic switch, and LD the polarisation-bistable laser diode

c Logic diagram and characteristic table of the S-R flip-flop

In our experimental demonstration of the S-R flip-flop operation, an alternative circuit shown in Fig. 2*b* was used, in which the two optoelectronic switches at the input ports were substituted with avalanche photodetectors (PD) because only one optoelectronic switch was available to us. The input signals, S and R, are generated by two AlGaAs/GaAs stripe geometry semiconductor lasers with pulsed current injection. The optical clock pulses are generated by an AlGaAs/GaAs transverse-junction-stripe laser driven by a train of current pulses. The optoelectronic switch consists of a Cr-doped semi-insulating GaAs substrate with a gap in the top metallisation. The switching efficiency was rather low (<1%) because the switch was not designed for this application. An amplifier was, therefore, used to enhance the electrical output of the optoelectronic switch before the signal was used to trigger the polarisation-bistable laser. As will be discussed later, the amplifier is not needed if well designed switches are used. The photographs in Fig. 3 show the operation of the optical S-R flip-flop.

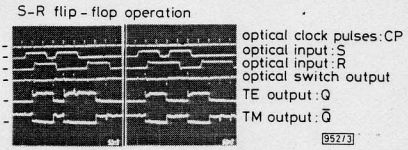

Fig. 3 *Operation of optical S-R flip-flop*

Trace 4 is the inverted electrical output switched out of the optoelectronic switch activated by the clock pulses. All other traces are optical signals

Limited by the speed of the pulse generators used to drive the semiconductor lasers which generated the S and R optical signals, we were not able to demonstrate subnanosecond operation of the flip-flop. However, an independent switching operation of the polarisation-bistable laser with short current pulses did show instrument-limited switching time in the order of 1 ns.[1] The response times of optoelectronic switches and photodetectors are a few hundred picoseconds. If very fast optical input signals are used, the overall switching speed of the flip-flop should be limited by the polarisation-bistable laser to <1 ns.

The scheme demonstrated in this letter is, in principle, operable at practical power levels of semiconductor lasers. Con-

sider optoelectronic switches made of semi-insulating GaAs with the following parameters: n (refractive index) = 3·6, $(\mu_n + \mu_p)$ (sum of electron and hole mobilities) = 2000 $cm^2V^{-1}s^{-1}$, l (the gap between electrodes) = 3 μm, $\hbar\nu$ (incident photon energy) = 1·5 eV and the conductance across the gap is[6] $G = 1 \times 10^{-2}\ \Omega^{-1}$/pJ. To switch the output of a polarisation-bistable laser within 1 ns, the current pulse needs to be 40 mA or 2 V across 50 Ω.[1] Such voltage can be delivered by the circuit with two optoelectronic switches connected in series shown in Fig. 2*a*, using 20 V DC bias and 2 pJ energy of the semiconductor laser pulse.

In conclusion, we have demonstrated the operation of a clocked optical S-R flip-flop based on polarisation-bistable semiconductor lasers with very simple circuitry. Other types of optical flip-flops can be constructed with similar schemes.

J. M. LIU
Y. C. CHEN

GTE Laboratories Incorporated
40 Sylvan Road
Waltham, MA 02254, USA

28th January 1985

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SHUNT-INDUCTANCE-COUPLED WAVEGUIDE FILTERS WITH EXPANDED SECOND STOPBAND

Indexing terms: Filters, Microwave filters

A computer-aided design is described for inductive iris and inductive double-strip coupled filters with increased-width resonator sections. The theory includes both the higher-order-mode interaction of all discontinuities and the finite thickness of the irises and inserts. The step-wall discontinuity effect is included in the optimisation process as an additional design parameter. Design examples for midband frequencies of about 11 and 16 GHz are given; the corresponding stopband attenuation is higher than 50 dB, or 40 dB, up to 18·5 GHz, or 24·5 GHz, respectively.

Introduction: Common rectangular waveguide bandpass filters coupled by inductive irises or *E*-plane integrated metal strips,[1–5] are composed of halfwave resonator sections equal in width to the feeding waveguide. Owing to the nonlinear relation between guide wavelength and frequency, however, for this type of filter, high attenuation requirements over a broad second stopband are often difficult to meet. To alleviate the problem, the cutoff frequency of the fundamental mode within the filter resonators may be suitably reduced by increasing the waveguide width in question. Moreover, the inductive junction effect of the step-wall discontinuity may be advantageously utilised as an additional design parameter for shunt-inductance coupled filters.

In this letter, therefore, inductive iris and inductive strip coupled resonator filters within an increased-width waveguide (Fig. 1) are investigated. As in References 3–5, the design of optimised filters is based on a rigorous field expansion technique into incident and scattered waves at all discontinuities. This allows direct inclusion of higher-order mode coupling, finite strip thickness and the step-wall discontinuity effects in the optimisation process.

Theory and design: The electromagnetic fields of each subregion at the corresponding discontinuities are derived from the x-component of the magnetic Hertzian vector,[3–5] which is

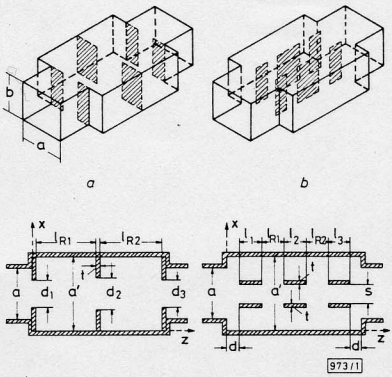

Fig. 1 *Shunt-inductance coupled filters with increased-width resonators*
a Inductive iris type
b Inductive double-strip type

assumed to be a sum of the eigenmodes satisfying the wave equation and the boundary conditions at the metallic surfaces:

$$\Pi_{hx} = \sum_{m=1}^{M} A_m^{\pm}\, T_m \sin\left[\frac{m\pi}{p} f\right] e^{\mp jk_{zm}z} \qquad (1)$$

where M is the number of eigenmodes considered, T_m is the normalisation factor so that the power carried by a given wave is 1 W for a wave amplitude of $1\sqrt{W}$,[3–5] p is the cross-section dimension (cf. References 3–5) of the subregions at the corresponding discontinuity considered, f is the variable in the x-direction (cf. References 3–5) of the subregion at the corresponding discontinuity considered, and $k_{zm}^2 = k^2 - (m\pi/p)^2$, $k^2 = \omega^2\mu\varepsilon$.

By matching the field components at the corresponding interfaces, the coefficients $A_m^{\pm}$ in eqn. 1 are determined after multiplication with the appropriate orthogonal function (cf. References 3–5). This yields the scattering matrix at the step discontinuity considered. The scattering matrix of the total filter is then calculated by directly combining the single scattering matrices, as in Reference 3. This procedure preserves numerical accuracy, since the direct combination of scattering matrix parameters contains exponential functions with only negative argument.

The computer-aided design is carried out by an optimising program[5] applying the evolution strategy method which varies the input parameters until the desired values of the insertion loss and of the stopband attenuation, for given bandwidths, are obtained. For additional given input and output waveguide housing dimensions a, b, thicknesses t of the irises or metal strips, respectively, spacing s of the double insert and number of resonators, the parameters to be optimised are the iris apertures d_i, or lengths l_i, of the double insert strips, respectively, the lengths l_{Ri} of the resonators, width a' of the increased width section, and distance d to the step discontinuity (for the double metal insert filter). For computer optimisation, the expansion into 15 eigenmodes at each discontinuity has turned out to be sufficient. The final design data are checked up by 35 eigenmodes.

Results: A five resonator Ku-band filter is chosen for the design example for the inductive irises coupled filter type (Fig. 1*a*). For comparison, Fig. 2 shows the calculated insertion loss $1/|S_{21}|$ in decibels for the usual iris filter (broken line), for the iris filter within a reduced-width waveguide (dash-dotted line), and for the iris filter within an increased-width waveguide (solid line). The curves demonstrate the better stopband attenuation behaviour of the increased-width filter.